Customer No.: 31561
Application No.: 10605,326
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IN THE CLAIMS

Please amend the claims as follows.

Claims 1-10 (canceled).

11. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate having a plurality of gate structures formed thereon, wherein each gate structure has a cap layer thereon;

performing an ion implantation for either implanting nitrogen ions into sidewalls of the gate structures or implanting oxygen or argon ions into exposed substrate between the gate structures; and

performing a thermal processing operation to form a liner layer on ~~the~~ sidewalls of the ~~conductive~~ gate structures and ~~the~~ exposed substrate, wherein ions implanted into the sidewalls of the gate structures suppress growth of the liner layer on the sidewalls of the gate structures and the ions implanted into the exposed substrate between the gate structures enhance growth of the liner layer on the exposed substrate so that the liner layer on the sidewalls of the ~~conductive~~ gate structures has a thickness smaller than the liner layer on the exposed substrate ~~surface~~.

12. (currently amended) The method of claim 11, wherein the step of performing an ion implantation furthermore comprises:

performing a tilt ion implantation for implanting ions into the sidewalls of the gate structures and the cap layers~~, wherein the implanted ions has a capability of inhibiting the growth of the oxide film during the thermal processing operation~~.

13. (original) The method of claim 11, wherein the ions implanted into the sidewalls of the gate structures comprises nitrogen ions.

Claim 14 (canceled).

15. (currently amended) The method of claim 14, wherein the ions implanted into the exposed substrate between the ~~neighboring~~ gate structures comprises oxygen ions or argon ions.

16. (original) The method of claim 11, wherein the step of forming the gate structures comprises:

forming a gate dielectric layer, a polysilicon layer, a metal silicide layer and a silicon nitride layer over the substrate;

patterning the silicon nitride layer; and

patterning the metal silicide layer and the polysilicon layer.

17. (currently amended) The method of claim 11, wherein before the step of performing the ion implantation, further comprises a step of performing a metal silicide etching operation to remove a portion of the ~~sidewall~~ metal silicide layer on sidewalls thereof.

18. (currently amended) The method of claim 11, wherein after the step of performing the ion implantation, further comprises a step of performing a metal

silicide etching operation to remove a portion of the ~~sidewall~~ metal silicide layer on sidewalls thereof.

19. (original) The method of claim 11, wherein the thermal processing operation comprises a step of performing a rapid thermal annealing operation followed by a rapid thermal oxidation.

20. (new) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate;

forming a plurality of gate structures, wherein a portion of the substrate is exposed between the gate structures;

implanting ions into the exposed substrate between the gate structures; and

performing a thermal processing operation to form a liner layer on sidewalls of the conductive structures and the exposed substrate, wherein the liner layer on the sidewalls of the gate structures has a thickness smaller than the liner layer on the exposed substrate.

21. (new) The method of claim 20, wherein the step of implanting ions into the exposed substrate comprises:

performing a vertical ion implantation for implanting oxygen or argon ions into the exposed substrate between the gate structures, wherein the oxygen or argon ions have a capability to enhance growth of the liner layer during the thermal processing operation.

22. (new) The method of claim 20, wherein the step of forming the gate structures comprises:

forming a gate dielectric layer, a polysilicon layer, a metal silicide layer and a silicon nitride layer over the substrate;

patterning the silicon nitride layer; and

patterning the metal silicide layer and the polysilicon layer.

23. (new) The method of claim 20, wherein before the step of implanting ions into the exposed substrate, further comprises a step of performing a metal silicide etching operation to remove a portion of the metal silicide layer on sidewalls thereof.

24. (new) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate having a plurality of gate structures formed thereon, wherein each gate structure has a cap layer thereon;

performing an ion implantation for either implanting nitrogen ions into sidewalls of the gate structures or implanting oxygen or argon ions into exposed substrate between the gate structures; and

performing a thermal processing operation to form a liner layer on sidewalls of the gate structures and exposed substrate, wherein nitrogen ions implanted into the sidewalls of the gate structures suppress growth of the liner layer on the sidewalls of the gate structures and the oxygen or argon ions implanted into the exposed substrate between the gate structures enhance growth of the liner layer on

the exposed substrate so that the liner layer on the sidewalls of the gate structures has a thickness smaller than the liner layer on the exposed substrate.

25. (new) The method of claim 24, wherein a tilt ion implantation process is carried out for implanting nitrogen ions into the sidewalls of the gate structures and a vertical ion implantation process is carried out for implanting oxygen or argon ions into the exposed substrate between the gate structures.

26. (new) The method of claim 24, wherein the step of forming the gate structures comprises:

forming a gate dielectric layer, a polysilicon layer, a metal silicide layer and a silicon nitride layer over the substrate;

patterning the silicon nitride layer; and

patterning the metal silicide layer and the polysilicon layer.